Notice of Allowability	Application No.	Applicant(s)	
	10/604,765	YANG ET AL.	
	Examiner	Art Unit	
	Stefan Stoynov	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *communication filed on August 14, 2003*.

2. ☒ The allowed claim(s) is/are *1-14*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

Pursuant to MPEP 606.01, change the title as follows:

Remove "[" and "]" at the beginning and the end of the title.

The title must read -- Method of State Maintenance for MMC Flash Storage Card in Communication Protocol --.

The following is an examiner's statement of reasons for allowance:

Byeon et al., U.S. Patent No. 6,882,570 discloses transitioning of a voltage detection signal during periods of temporary voltage drop (column 7, lines 58-67, column 8, lines 1-2, FIG. 3A-3C). In addition, Byeon discloses generation of a power-on reset signal that follows the power supply voltage, a detection signal, and a power-on read signal in response to the power-on reset signal and the detection signal (column 11, lines 1-9). In Byeon, generating the above-mentioned power-on read signal prevents unnecessary read operations during power supply noise fluctuations (Abstract).

Ishikuri, U.S. Patent No. 6,674,681 discloses a low voltage detection circuit used for determining whether the voltage has fallen bellow a level in which the RAM may

reliably hold data and preventing further memory access during this state, thus ensuring data integrity (column 9, lines 22-45).

Kuddes et al., U.S. Patent No. 5,717,907 discloses a reset generating circuit used for placing a microprocessor into a known state upon power-up when power fluctuations occur (column 1, lines 12-17).

Applicant's admitted prior art teaches activating and deactivating of low voltage detection (LVD) signal based on supply voltage level and a reset signal changing in correspondence with the LVD signal.

Re claim 1, the prior art of record does not teach or suggest, individually or in combination, "using an LVD interrupt signal to interrupt data transferring or receiving, wherein when the LVD signal changes from the first state to the second state, the LVD interrupt signal is issued; and resetting the LVD interrupt signal, when the LVD signal changes from the second state to the first state, and the LVD interrupt signal is indeed polled by a firmware".

Re claim 9, the prior art of record does not teach or suggest, individually or in combination, "a firmware polling signal, to poll the LVD interrupt signal when the LVD interrupt has changed from the first state to the second state; and an LVD interrupt reset signal, which is issued after the LVD signal has changed from the low-voltage state back to the normal state and the LVD interrupt signal is indeed polled by the firmware polling signal, wherein the LVD interrupt reset signal resets the LVD interrupt signal".

Re claim 13, the prior art of record does not teach or suggest, individually or in combination, "an LVD interrupt reset signal, which is issued after the LVD signal has

changed from the low-voltage state back to the normal state, wherein the LVD interrupt reset signal resets the LVD interrupt signal".

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stefan Stoynov whose telephone number is (571) 272-4236. The examiner can normally be reached on 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

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